Digital signals produce pure sine waves

RONALD MANCINI, HARRIS SEMICONDUCTOR, MELBOURNE, FL

Analog oscillators produce excellent sine waves but are temperamental and hard to design. They also require extensive redesign every time you change the oscillation frequency. Digital oscillators are easier to design than analog oscillators, and digital signals already exist in digital systems. Thus, it is often cost-effective to derive sine waves from digital signals.

For example, a simple circuit can derive a sine wave with a frequency 1/32 of the input from almost any periodic digital-input signal (**Figure 1**). The counter chain acts as a frequency divider and works with the digital-input signal to determine the output sine wave's frequency. A 5-bit counter divides the digital signal by 32. In addition to producing the desired frequency for the application, dividing by 32 separates the digital-noise and switching steps from the sine-wave frequency by the same factor, making it easier to filter the sine wave. The more stages in the counter, the higher the frequency separation between the digital input and output sine wave and the easier the filtering job is.

The counter output connects to the serial input of the shift register and determines the patterns of ones and zeros that shift down the register. Because the counter in this case is 5 bits, 16 ones shift into the register followed by 16 zeros. The 16 ones make up the rising part of the sine wave, and the 16 zeros make up the falling part of the sine wave. Assume that all shift-register outputs are low. Now, the parallel combination of all the resistors acts as a termination to the digital low level that serves as ground. The first shift-register output, Q_A, connects to a 51-kΩ resistor, and when Q_A goes to a high state, the resistor slightly pulls up the junction voltage. Each succeeding resistor that connects to the succeeding shift-register output pulls up the junction voltage in steps until all of the shift-register outputs are high. When the shift register's serial input waveform goes low, zeros shift into the shift-register output, and the process reverses to form the sine wave's decreasing portion.

The resistor weights are sinusoidal. Therefore, the output voltage takes small steps when a sine wave has a slow rising or falling voltage. Resistor weighting ensures that the voltage steps are larger when the sine-wave voltage should have a fast rising/falling voltage. Note that the resistors are symmetrical about one-fourth of the period to ensure that the rising and falling curves of the sine wave are symmetrical.

If you increase the counter to 6 bits, the output sine wave is 1/64 of the input signal, the resistors and shift registers double, and sine wave's purity dramatically increases. If you use CMOS for the digital circuits, no pullup resistors are necessary, but bipolar digital circuits require pullup resistors to ensure that the high level stays close to the supply rail.

The output filter is a second-order lowpass filter with a cutoff frequency of 100 kHz. This frequency enables the circuit to deliver a clean 86-kHz sine-wave output with a 2.78-MHz digital input. This filter prevents any discernible switching glitches or voltage steps on the output. If the counter is only 4 bits, however, some of the digital noise from the stepped sine wave appears on the output sine wave. (DI #2096)

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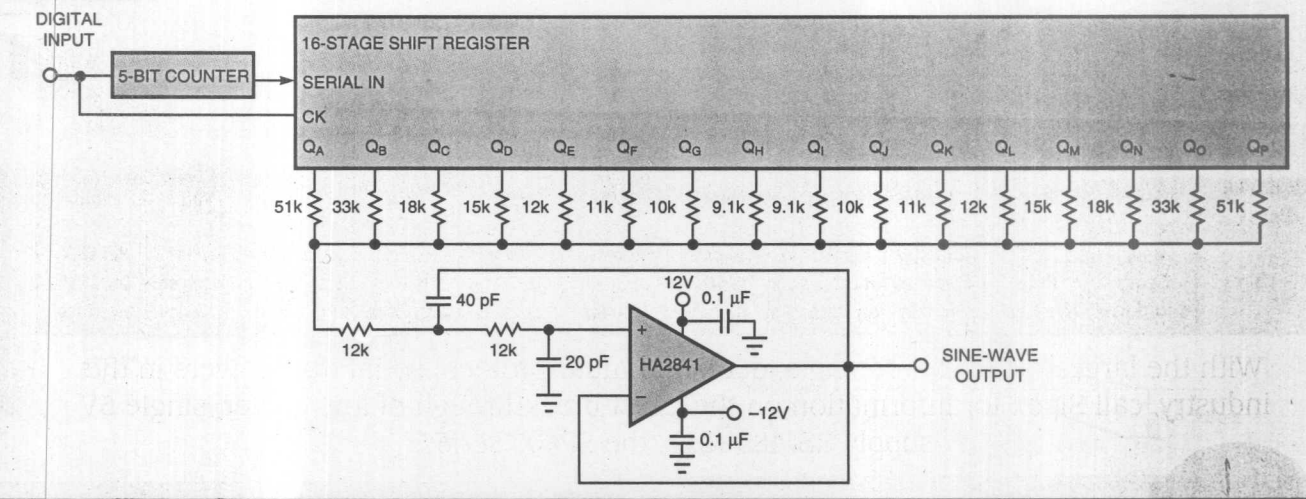
FIGURE 1



A 5-bit counter, a 16-stage shift register, appropriately weighted resistors, and a second-order filter produce a clean 86-kHz sine wave from a 2.78-MHz digital input.